

Dr. John A Curreri

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US citizen

PROFESSIONAL EXPERIENCE

Intel

Senior Validation Engineer, March 2011 – Aug 2026

Columbia Design Center (CDC) and Austin site

- Validated the coherency and on-die interconnect of 12 generations of server CPUs.
- Performed both pre-si (emulation) and post-si validation in a Linux based debug environment.
- Used Visual Studio Code to develop automatic AI agentic failure binning flows

University of Florida

Research Assistant, May 2005 – March 2011

NSF CHREC (Center for High- Performance Reconfigurable Computing)

- Performed research for the Translation and Execution Productivity Group under Dr. George.
- Conducted dissertation research to increase execution productivity with High-Level Synthesis tools.
- Developed and evaluated a novel runtime performance analysis and verification tool.

HCS (High-Performance Computing and Simulation) Lab

- Performed research for the Advance Space Group under Dr. George.
- Successfully demonstrated new satellite architecture for NASA's New Millennium Project.
- Developed middleware critical to the satellites' fault tolerance and performed timing of error propagation

PERSONAL EXPERIENCE

Metrology

- Developed AI-assisted automation for precision metrology equipment including nanovolt meters, frequency counters, potentiostats, LCR meters, and calibration standards using SCPI and Python.

TECHNICAL SKILLS

AI

- Prompt engineering, AI agents running looping and graph agentic flows, Local LLMs running on vLLM, MCP
- Platform: RTX 6000 Pro running Qwen 3.6 27B

Hardware

- FPGA Platforms: Cray XD1, XtremeData XD1000, SRC 7, Nallatech H100 (past graduate work)
- Microprocessors: MSP430, ATmega, ARM (hobby development boards), Intel x86 (server validation)
- Languages: VHDL, Verilog (written for past graduate work and read for intel validation)
- Environments: Xilinx ISE, Altera Quartus, Impulse C, Carte C, Dime Talk (past graduate work)

Software

- Languages: C, C++, Python (current during Intel validation)

EDUCATION

University of Florida

Ph.D., Computer Engineering, April 2011, **GPA: 3.9**

University of Florida

Master of Science, Computer Engineering, December 2006, **GPA: 3.9**

University of Alabama in Huntsville

Bachelor of Science, Computer Engineering, Mathematics, May 2005, **GPA: 3.977**

SELECTED PUBLICATIONS

Published internal DTTC (Design and Test Technology Conference) paper at Intel, 2013

J. Curreri, S. Koehler, A. George, B. Holland, and R. Garcia, 'Performance Analysis Framework for High-Level Language Applications in Reconfigurable Computing,' ACM Transactions on Reconfigurable Technology and Systems (TRETS), 3, 1 (Jan. 2010), 1-23.

J. Curreri, G. Stitt, and A. D. George, "High-level Synthesis of In-Circuit Assertions for Verification, Debugging, and Timing Analysis," International Journal of Reconfigurable Computing (IJRC), vol. 2011, Article ID 406857, 17 pages, 2011, doi:10.1155/2011/406857.